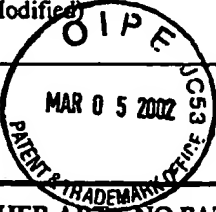


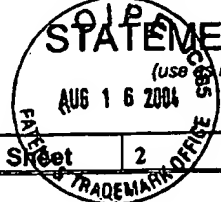
Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 04259.P044	Application Number: 09/954,915
		First Named Inventor: Mark Peting	RECEIVED MAR 08 2002 Technology Center 2600
		Filing Date: September 17, 2001	
OTHER ART - NO PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
KT		JAMES TSUI, Frequency Channelization, Digital Techniques for Wideband Receivers, Second Edition, Pages 363 - 396, 2001 Artech House, Inc., Norwood, MA, <i>Dec 2003</i>	
		ZHENGDAO WANG and GEORGIOS B. GIANNAKIS, Wireless Multicarrier Communications where Fourier Meets Shannon, Department of ECE, University of Minnesota, Minneapolis MN., Pages 1-21, <i>May 2000</i>	
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		G.A. SHAW, R.A. FORD, J.C. ANDERSON, B.W. ZUERDORFER, A.H. ANDERSON, RASSP Benchmark 2 Technical Description, Massachusetts Institute Of Technology Lincoln Library, 153 pages total, <i>10 August 1995</i>	
		"www.inventra.com/inventra/softcore/workshop/MultiRaFiltDes95/", MENTOR GRAPHICS, Hardware Design of Decimators/Interpolators, Pages 1-38, <i>2006</i>	
KT		"www.mentor.com/inventra/softcore/workshop/SDmod95/", MENTOR GRAPHICS, Introduction to AD/DA Converters, Pages 1-27, <i>2006</i>	
		http://www.mentor.com/inventra/softcore/workshop/SDHWDes95/ MENTOR GRAPHICS, Design of the Decimation & Interpolation Filters, Pages 1-57, <i>2007</i>	
		http://www.mentor.com/inventra/softcore/workshop/Applications95/, MENTOR GRAPHICS, Sigma Delta Converter Applications, Pages 1-5, <i>2007</i>	

Examiner Signature	/Khai Tran/	Date Considered	11/08/2006
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

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Substitute for Form 1449/PTO				Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	09/954,915
				Filing Date	September 17, 2001
				First Named Inventor:	Mark Peting
				Art Unit	2661
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	004259.P04 Technology Center 2600
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
KT ↓ KT		BREE, ET AL., "A Bit-Serial Architecture For A VLSI Viterbi Processor", Communications Systems Research Group, University of Saskatchewan, Saskatoon, IEEE, WESCANEX '88, 1988, pages 72-77.			
		BIVER, ET AL., "Architectural Design and Realization Of A Single-Chip Viterbi Decoder", Elsevier Science Publishers B.V., INTEGRATION, The VLSI Journal 8 (1989), October, No. 1, Amsterdam, NL, Pages 3-16.			
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		CHOI, ET AL., "Viterbi Detector Architecture For High-Speed Optical Storage", 1997, IEEE TENCON - Speech and Image Technologies for Computing and Telecommunications, ASIC Center Corporate Technical Operations SAMSUNG Electronics, Vol. 1, Dec 1997, pages 89-92.			
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		HASHIDA MITSUYOSHI, "Hierarchical Network Management System and Control Method for Network Management Information," Patent Abstracts of Japan, Publication No. 07226777, 2006			

Examiner Signature	/Khai Tran/	Date Considered	11/08/2006
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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